Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A0**
2. **ENABLE**
3. **V-**
4. **S1**
5. **S2**
6. **S3**
7. **S4**
8. **D**
9. **S8**
10. **S7**
11. **S6**
12. **S5**
13. **V+**
14. **GND**
15. **A2**
16. **A1**

**.045”**

**1 16**

**2**

**3**

**4**

**5**

**6**

**7**

**8 9**

**15**

**14**

**13**

**12**

**11**

**10**

**MASK**

**REF**

**SCIY**

**A**

**.077”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .0035 x .0035”**

**Backside Potential: -V or FLOAT**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .045” X .077” DATE: 9/23/21**

**MFG: SILICONIX THICKNESS .015” P/N: DG508A**

**DG 10.1.2**

#### Rev B, 7/1